SHENZHEN TIBTRONIX TECHNOLOGY CO., LTD.

T8PLHG80D

100Gb/s ZR4 80km QSFP28 Transceiver Hot Pluggable, Duplex LC Connector, Single mode

2022/1/18

Shenzhen Tibtronix Technology Co., Ltd.

3/F,12th Building, Nangang 1st Industrial Park, Baimang Xili, Songbai Road, Nanshan District, Shenzhen, China

Tel: +86 755 23316583 Fax: +86 755 29810056 E-mail: sales@tibtronix.com http://www.tibtronix.com

Features:

- ✧ 4 LAN-WDM lanes MUX/DEMUX design
- ✧ QSFP28 MSA compliant
- ✧ Hot pluggable 38 pin electrical interface
- ✧ 4x25G electrical interface
- ✧ Up to 80km transmission on single mode fiber
- ✧ Supports 103.125Gb/s aggregate bit rat
- ✧ Aggregate bandwidth of > 100Gbps
- ✧ Duplex LC connectors
- ✧ Single +3.3V power supply operating
- ✧ Temperature range 0°C to 70°C
- ✧ RoHS 2.0 Compliant Part
- ✧ Maximum power consumption 6.5W

Applications:

- ✧ 100GBASE-ZR4 100G Ethernet
- ✧ Telecom networking

Description:

The T8PLHG80D is a transceiver module designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wire serial interface. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. A block diagram is shown in Figure 1.

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	T_S	-40		+85	°C
Supply Voltage	$V_{CC}T$, R	0		3.6	V
Relative Humidity	RH	15		85	%
Damage Threshold, each lane	THd	6.5			dBm

Notes
1. Non-condensing

Recommended Operating Environment:

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	T_C	0		+70	°C
Supply Voltage	$V_{CCT, R}$	+3.13	3.3	+3.47	V
Supply Current	I_{CC}		1100	1960	mA
Power Dissipation	PD			6.5	W
Link Distance with G.652				80	km

Electrical Characteristics (T_{OP} = 0 to 70 °C, VCC = 3.13 to 3.47 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Consumption		-		6.5	W	
Supply Current	Icc	-		1.960	A	Steady state
Transmitter						
Data Rate per Channel			25.78125		Gbps	
Differential Voltage pk-pke	Vpp			900	mV	At 1 MHz
Common mode Voltage Tolerance	Vcm	-350		2850	mV	
Transition time	Trise/Tfall	10			ps	
Transmit Input Diff Impedance	ZIN	85	100	115		20%~80%
Differential Termination Resistance Mismatch				10	%	

Eye width	EW15	0.46			UI	
Eye height	EH15	95			mV	
Receiver						
Data Rate per Channel			25.78125		Gbps	
Differential Termination Resistance Mismatch				10	%	At 1 MHz
Differential output voltage swing	Vpp			900	mV	
Common mode Voltage Tolerance	Vrms			17.5	mV	
Transition time	Trise/Tfall	12			ps	
Eye width	EW15	0.57			UI	
Eye height	EH15	228			mV	

● Optical Parameters(EOL,TOP = 0 to +70 ˚C, VCC = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Signaling Speed per Lane		25.78125 ± 100 ppm			Gb/s	
Wavelength Assignment	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Side-mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	PT	8	-	12.5	dBm	
Average Launch Power, each Lane	TXPx	2	-	6.5	dBm	
Difference in Launch Power between any two Lanes (OMA)		-	-	3	dB	
Extinction Ratio	ER	6	-	-	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Optical Return Loss Tolerance		-	-	20	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Relative Intensity Noise	Rin			-130	dB/HZ	1
Optical Return Loss Tolerance		-	-	-12	dB	
Mask margin		5			%	
Receiver						
Signaling Speed per Lane		25.78125 ± 100 ppm			Gb/s	

Wavelength Assignment	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Damage Threshold	THd	6.5			dBm	
Average receiver power, each lane		-28		2	dBm	
Receiver Power (OMA), each Lane	OMA	-	-	-4.5	dBm	
Receiver Sensitivity (OMA) per Lane	Rxsens			-28	dBm	1
Receiver 3 dB electrical upper cut off frequency, each lane				31	GHz	
Receiver Reflectance	Rrx			-26	dB	
LOS De-Assert	LOSD	-	-	-29	dBm	
LOS Assert	LOSA	-40	-	-	dBm	
LOS Hysteresis	LOSH	0.5	-	-	dB	
Link Budget			-31		dB	

Note

1. Sensitivity is specified at BER@10E-5 with FEC

● Diagnostic Monitoring Interface

T8PLHG80D support the I2C-based Diagnostic Monitoring Interface (DMI) defined in document SFF-8636. The host can access real-time performance of transmitter and receiver optical power, temperature, supply voltage and bias current.

Performance Item	Related Bytes(A0[00] memory)	Monitor Error	Notes
Module temperature	22 to 23	+/-3°C	1，2
Module voltage	26 to 27	< 3%	2
LD Bias current	42 to 49	< 10%	2
Transmitter optical power	50 to 57	< 3dB	2
Receiver optical power	34 to 41	< 4dB	2

Note

1. Actual temperature test point is fixed on module case around Laser.
2. Full operating temperature range.

EEPROM Definitions

Lower Memory Map

Address	Type	Size	Name	Description	Value(Hex)	Remarks
0	R	1	Identifier	Identifier		
1	R	1	Status	Revision Compliance		
2	R	1	Status	Flat_mem/ IntL/Data_Not_Ready		
3	R	1	Interrupt Flags	Latched TX/RX LOS indicator		
4	R	1		Latched TX Adaptive EQ/TX Transmitter/Laser fault indicator		
5	R	1		Latched TX/RX CDR LOL indicator		
6	R	1		Latched temperature A/W / Initialization complete flag		
7	R	1		Latched supply voltage A/W		
8	R	1		Vendor Specific		
9~10	R	2		Latched RX power A/W		
11~12	R	2		Latched TX bias A/W		
13~14	R	2		Latched TX power A/W		
15~18	R	4		Reserved		
19-21	R	2		Vendor Specific		
22-23	R	2	Device monitors	Module temperature		
24-25	R	2		Reserved		
26-27	R	2		Supply voltage		
28-29	R	2		Reserved		
30-33	R	4		Vendor Specific		
34-35	R	2	Power monitors	RX input power, channel 1		
36-37	R	2		RX input power, channel 2		
38-39	R	2		RX input power, channel 3		
40-41	R	2		RX input power, channel 4		
42-43	R	2	LD Bias Monitors	TX bias, channel 1		
44-45	R	2		TX bias, channel 2		

Address	Type	Size	Name	Description	Value(Hex)	Remarks
46-47	R	2		TX bias, channel 3		
48-49	R	2		TX bias, channel 4		
50-51	R	2	Power monitors	TX power, channel 1		
52-53	R	2		TX power, channel 2		
54-55	R	2		TX power, channel 3		
56-57	R	2		TX power, channel 4		
58-73	R	16		Reserved		
74-81	R	8		Vendor Specific		
82-85	R	4		Reserved		

86	RW	1	Control	Tx Disable		
87	RW	1		Rx_Rate_select		
88	RW	1		Tx _Rate_select		
89~92	RW	4		Rx_Application_Select		
93	RW	1		Power		
94~97	RW	4		Tx_Application_Select		
98	RW	1		TX/RX CDR_control		
99	RW	1		Reserved		
100-104	RW	4	Free Side Device and Channel Masks	Module and Channel Masks		
105	RW	1		Vendor Specific		
106	RW	1		Vendor Specific		
107	RW	1		Reserved		
108-109	R	2	Free Side Device Properties	Most significant byte of propagation delay		
110	R	1		Advanced Low Power Mode / Far Side Managed / Min Operating Voltage		
111-112	RW	2	Assigned for use by PCI Express	PCI		
113	R	1	Free Side Device Properties	End Implementation		

Address	Type	Size	Name	Description	Value(Hex)	Remarks
114-118	RW	6		Reserved		
119-122	W	4		Password Change Entry Area		
123-126	W	4		Password Entry Area		
127	RW	1		Page Select Byte		

Upper Memory Map Page 00h

Address	Type	Size	Name	Description	Value(Hex)	Remarks
128	R	1	Identifier	Identifier Type of serial Module		
129	R	1	Ext. Identifier	Extended Identifier to free side device. Includes power classes, CLEI codes, CDR capability		
130	R	1	Connector	Code for connector type		
131	R	1	Specification compliance	10/40G/100G Ethernet Compliance Codes		
132	R	1		SONET Compliance Codes		
133	R	1		SAS/SATA Compliance Codes		
134	R	1		Gigabit Ethernet Compliant Codes		
135~136	R	1		Fibre Channel link length/Fibre Channel Transmitter Technology		
137	R	1		Fibre Channel transmission media		
138	R	1		Fibre Channel Speed		
139	R	1	Encoding	Code for serial encoding algorithm		
140	R	1		Nominal bit rate, units of 100Mbps. For BR>25.4G, set this to FFh and use Byte 222.		
141	R	1		QSFP+ Rate Select Version 2.		
142	R	1		Link length supported for SMF fiber in km		
143	R	1	Length	Length(OM3 50um)		
144	R	1		Length(OM2 50um)		
145	R	1		Length(OM1 62.5 um)		
146	R	1		Length(OM5 50um)		
147	R	1	Device tech-nology	Device technology		

Address	Type	Size	Name	Description	Value(Hex)	Remarks
148	R	1	Vendor name	Free side device vendor		
149	R	1				
150	R	1				
151	R	1				
152	R	1				
153	R	1				
154	R	1				
155	R	1				
156	R	1				
157	R	1				
158	R	1				
159	R	1				
160	R	1				
161	R	1				
162	R	1				
163	R	1				
164	R	1	Extended Module			
165~167	R	1	Vendor OUI			
168	R	1	Vendor PN	Part number provided by free side device vendor		
169	R	1				
170	R	1				
171	R	1				
172	R	1				
173	R	1				
174	R	1				
175	R	1				
176	R	1				
177	R	1				

Address	Type	Size	Name	Description	Value(Hex)	Remarks
178	R	1				
179	R	1				
180	R	1				
181	R	1				
182	R	1				
183	R	1				
184	R	1	Vendor rev	Revision level for part number provided by vendor		
185	R	1				
186	R	1	Wavelength	Nominal laser wavelength (wave-length=value/20 in nm)		
187	R	1				
188	R	1	Wavelength tolerance	Guaranteed range of laser wave-length(+/- value) from nominal wave-length. (wavelength Tol.=value/200 in nm)		
189	R	1				
190	R	1	Max case temp	Maximum case temperature in degrees C		
191	R	1	C_BASE	Check code for base ID fields		
192	R	1	Link codes	Extended Specification Compliance Codes		
193	R	1	Options	TX Input Equalization Auto Adaptive Capable not implemented, TX Input Equalization Fixed Program-mable Settings implemented, RX Output Emphasis Fixed Programma-ble Settings implemented, RX Output Amplitude Fixed Program-mable Settings implemented		
194	R	1		Tx CDR LOL Flag, Rx CDR LOL Flag, RX Squelch Disable, RX Output Disable, TX Squelch Disable, TX Squelch		

Address	Type	Size	Name	Description	Value(Hex)	Remarks
195	R	1		Memory page 02h implemented, Memory page 01h implemented, Active control of the select bits in the upper memory table is required to change rates, Tx_DISABLE and serial output implemented, Tx_FAULT signal implemented, Tx Loss of Signal implemented		
196	R	1	Vendor SN	Serial number provided by vendor		
197	R	1				
198	R	1				
199	R	1				
200	R	1				
201	R	1				
202	R	1				
203	R	1				
204	R	1				
205	R	1				
206	R	1				
207	R	1				
208	R	1				
209	R	1				
210	R	1				
211	R	1				
212	R	1	Date Code	Vendor's manufacturing date code		
213	R	1				
214	R	1				
215	R	1				
216	R	1				
217	R	1				

Address	Type	Size	Name	Description	Value(Hex)	Remarks
218	R	1				
219	R	1				
220	R	1	Diagnostic Monitoring Type	Average RX power measurement, Transmitter power measurement supported		
221	R	1	Enhanced Options	Indicates which optional enhanced features are implemented (if any) in the free side device.		
222	R	1	BR, nominal	Nominal bit rate per channel, units of 250Mbps.		
223	R	1	CC_EXT	Check Code for Address 192 to 222		
224	R	1				
225	R	1				
226	R	1				
227	R	1				
228	R	1				
229	R	1				
230	R	1				
231	R	1	Vendor Specific			
232	R	1				
233	R	1				
234	R	1				
235	R	1				
236	R	1				
237	R	1				
238	R	1				
239	R	1				
240	R	1	Vendor Specific			
241	R	1				
242	R	1	Vendor Specific			
243	R	1		Reserved		

Address	Type	Size	Name	Description	Value(Hex)	Remarks
244	R	1				
245	R	1				
246	R	1				
247	R	1				
248	R	1				
249	R	1				
250	R	1	Checksum			
251	R	1	Vendor Specific			
252	R	1				
253	R	1				
254	R	1				
255	R	1				

● Alarm and Warning Thresholds

T8PLHG80D support alarms function, indicating the values of the preceding basic performance are lower or higher than the thresholds.

Performance Item	Alarm Threshold Bytes(A0[03] memory)	Unit	Low threshold	High threshold
Temp Alarm	128 to 131	℃	-10	80
Temp Warning	132 to 135	℃	0	70
Voltage Alarm	144 to 147	V	2.97	3.63
Voltage Warning	148 to 151	V	3.135	3.465
TX Power Alarm	192 to 195	dBm	-4	8.2
TX Power Warning	196 to 199	dBm	-1	6.5
RX Power Alarm	176 to 179	dBm	-31	-4
RX Power Warning	180 to 183	dBm	-28	-7

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode =Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	toff_IntL 500 μs Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower Power Level

Power_over-ride or Power-set De-assert Time	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module is fully functional3

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

● Transceiver Block Diagram

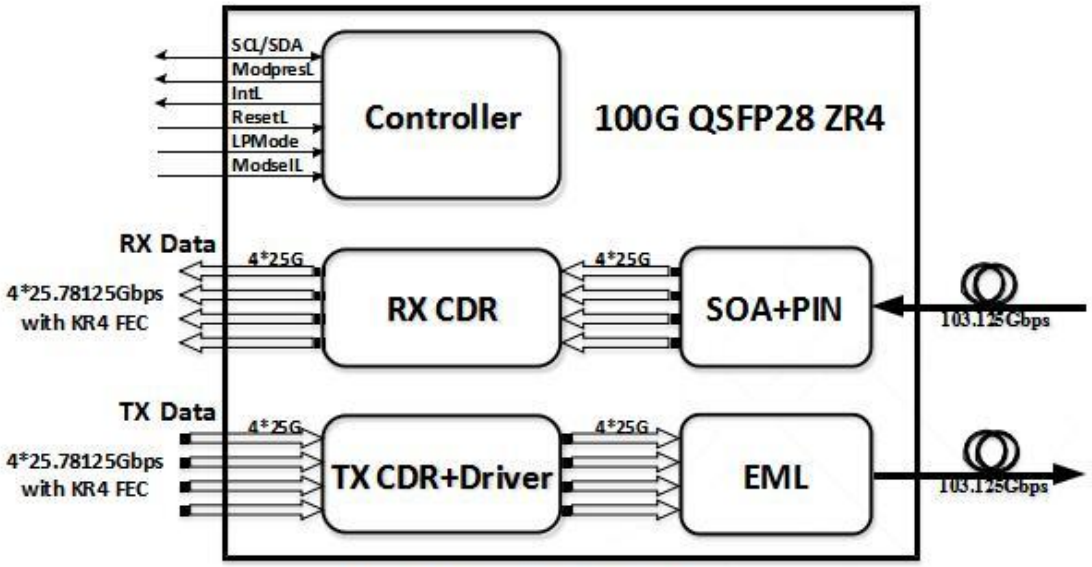

Figure 1. Transceiver Block Diagram

● Pin Assignment

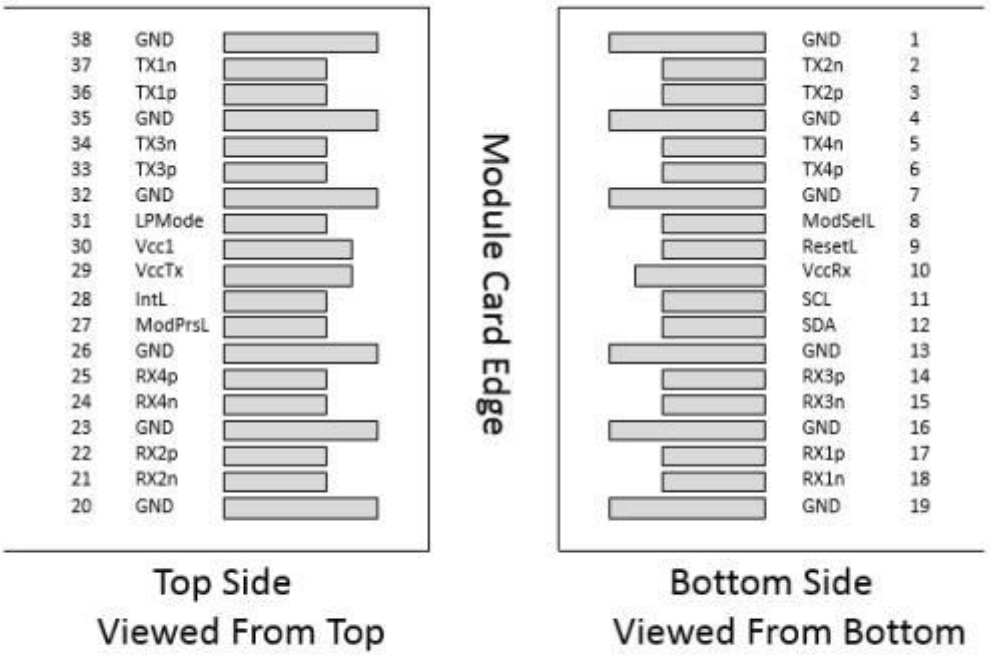

Figure 2. MSA compliant Connector

● Pin Description

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1

17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for single and supply(power) common for QSFP28 modules, All are common within the QSFP28 module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

Mechanical Dimensions

Tibtronix's T8PLHG80D 100G ZR4 QSFP28 transceivers are compatible with the QSFP28 Specification for pluggable form factor modules.

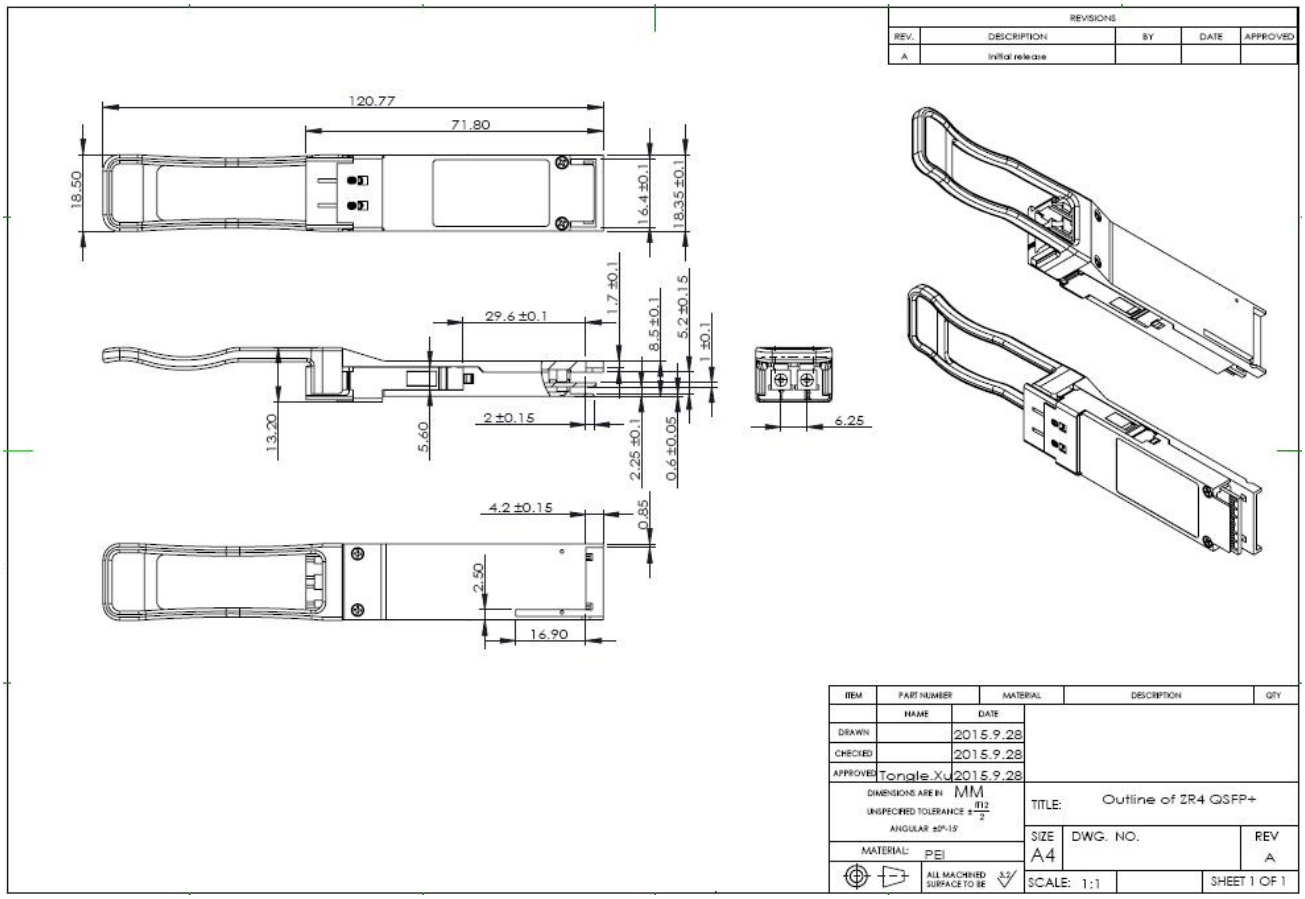

Figure 3. Mechanical Dimensions

ESD Design

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected

environment utilizing standard grounded benches, floor mats, and wrist straps.

Parameter	Threshold value	Notes
ESD of high-speed pins	1KV	Human Body Model
ESD of low-speed pins	2KV	Human Body Model
Air discharge during operation	15KV	
Direct contact discharges to the case	8KV	