TIBTRONIX TECHNOLOGY CO., LTD.

T8BLHG80D4-2804&0482

100Gb/s QSFP28 BiDi 80km Transceiver Hot Pluggable, Simplex LC Connector, EML+PIN with SOA Single mode DDM

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Features:

- ✧ 4x25Gb/s LAN WDM Blue or Red Side TOSA, LAN WDM Red or Blue Side ROSA with SOA
- ✧ Support 100GBASE-ZR4 for line rate of 103.125Gbps and OTU4 for line rate of 111.81Gbps
- ✧ Compliant with IEEE 802.3-2012 Clause 88 standard IEEE 802.3bm CAUI-4 chip to module electrical standard ITU-T G.959.1-2012-02 standard
- ✧ Simplex LC connector
- ✧ Single +3.3V power supply operating
- ✧ Temperature range 0° C to 70° C
- ✧ RoHS Compliant Part

Applications:

- ✧ 100GBASE-ZR4
- ✧ Data Center

Description:

TIBTRONIX's T8BLHG80D4 provides 100GBase-BX throughput up to 80km over single-mode fiber (SMF) using wavelengths of 1273.54, 1277.89, 1282.26, 1286.66nm- TX/1295.56, 1300.05, 1304.58, 1309.14nm-RX(1295.56, 1300.05, 1304.58, 1309.14nm- TX/1273.54, 1277.89, 1282.26, 1286.66nm-RX) via an LC connector. This bidirectional unit must be used with another transceiver or network appliance of complimenting wavelengths. Digital diagnostics functions are also available via the I2C interface, as specified by the QSFP28 MSA, to allow access to real-time operating parameters. With these features, this easy to install, hot swappable transceiver is suitable to be used in various applications, such as 100G Ethernet, data center, and storage area networks applications.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	T_S	-40		+85	°C
Supply Voltage	$V_{CC}T$, R	-0.5		4	V
Relative Humidity	RH	0		85	%

Recommended Operating Environment:

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	T_C	0		+70	°C
Supply Voltage	$V_{CCT, R}$	+3.13	3.3	+3.47	V
Supply Current	I_{CC}		1200	1900	mA
Power Dissipation	PD			6.5	W

Electrical Characteristics (T_{OP} = 0 to 70 °C, VCC = 3.13 to 3.47 Volts

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data Rate per Channel		-	25.78125		Gbps	
			27.9525			
Power Consumption		-	4	6.5	W	
Supply Current	Icc		1.2	1.8	A	
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			35	Ps	
RESETL Duration			10		Us	
RESETL De-assert time				100	ms	
Power On Time				100	ms	
Transmitter						
Single Ended Output Voltage Tolerance		0.3		Vcc	V	1
Common mode Voltage Tolerance		15			mV	
Transmit Input Diff Voltage	VI	150		1200	mV	
Transmit Input Diff Impedance	ZIN	85	100	115		
Data Dependent Input Jitter	DDJ		0.3		UI	
Receiver						
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	Vo	370	600	950	mV	
Rx Output Rise and Fall Voltage	Tr/Tf			35	ps	1

Total Jitter	TJ		0.3		UI	

Note:

1. 20～80%

● Optical Parameters(TOP = 0 to 70 °C, VCC = 3.0 to 3.6 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Purple Side Four Lane Wavelength Range	λ1	1272.54	1273.54	1274.54	nm	
	λ2	1276.89	1277.89	1278.89	nm	
	λ3	1281.25	1282.26	1283.27	nm	
	λ4	1285.65	1286.66	1287.68	nm	
Write Side Four Lane Wavelength Range	λ1	1294.56	1295.56	1296.56	nm	
	λ2	1299.05	1300.05	1301.05	nm	
	λ3	1303.58	1304.58	1305.58	nm	
	λ4	1308.14	1309.14	1310.14	nm	
Side-mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	PT	8	-	12.5	dBm	
Average Launch Power, each Lane		+2	-	6.5	dBm	
Difference in Launch Power between any two Lanes (OMA)		-	-	3	dB	
Extinction Ratio	ER	6	-	-	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				1
Optical Return Loss Tolerance		-	-	20	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Relative Intensity Noise	Rin			-130	dB/HZ	
Optical return loss tolerance				20	dB	
Transmitter reflectance		-	-	12	dB	
Receiver						
Purple Side Four Lane Wavelength Range	λ1	1272.54	1273.54	1274.54	nm	
	λ2	1276.89	1277.89	1278.89	nm	
	λ3	1281.25	1282.26	1283.27	nm	
	λ4	1285.65	1286.66	1287.68	nm	
Write Side Four Lane Wavelength Range	λ1	1294.56	1295.56	1296.56	nm	
	λ2	1299.05	1300.05	1301.05	nm	
	λ3	1303.58	1304.58	1305.58	nm	

	λ4	1308.14	1309.14	1310.14	nm	
Total Damage Threshold	THd			5.5	dBm	1
Receiver Sensitivity per Lane	R			-28	dBm	
Average Power at Receiver Input, each Lane	R	-28		0	dBm	1
LOS De-Assert	LOS_D			-29	dBm	
LOS Assert	LOS_A	-40			dBm	
LOS Hysteresis	LOS_H	0.5			dB	

Note

1. Sensitivity is specified at BER@5E-5 with FEC

● Timing for Soft Control and Status Functions

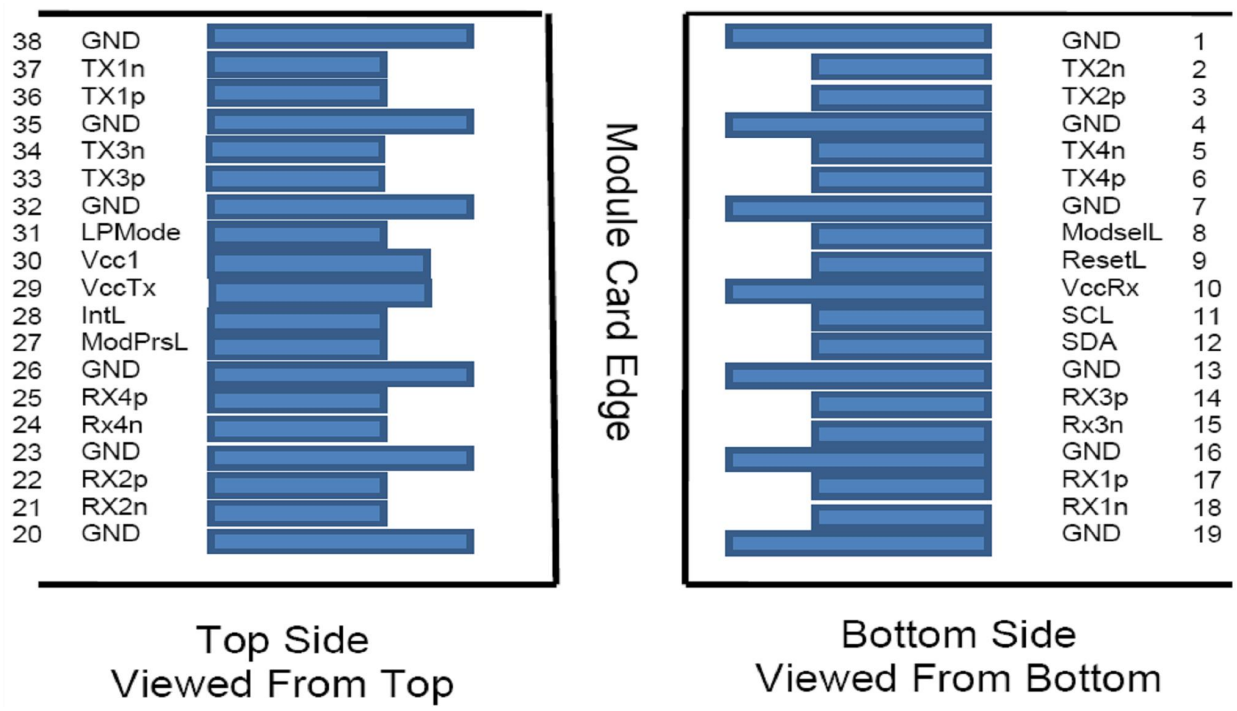
Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode =Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	toff_IntL 500 μs Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL

				assertion is inhibited
Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower Power Level
Power_over-ride or Power-set De-assert Time	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module is fully functional3

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

● Pin Assignment



Pin Description

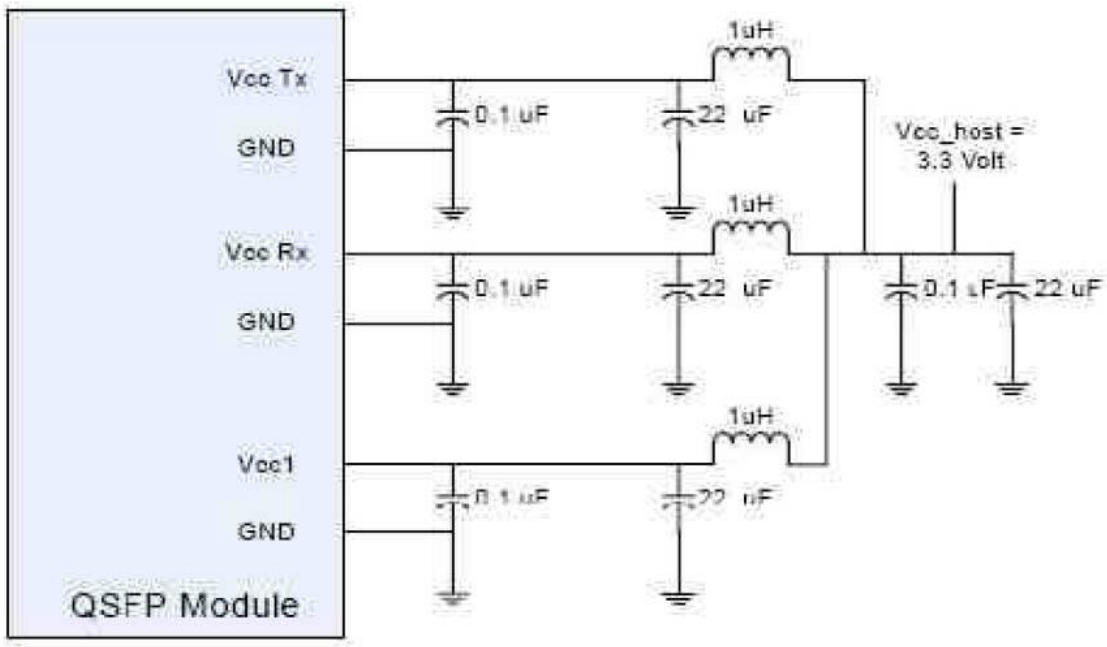
Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	

37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for single and supply(power) common for QSFP28 modules, All are common within the QSFP28 module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

Recommended Circuit



Mechanical Dimensions